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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/934,495	08/22/2001	Nobuo Mamada	3246/FLK/DIV of 2798/FLK	8056

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EXAMINER	
GOFF II, JOHN L	

ART UNIT	PAPER NUMBER
1733	

DATE MAILED: 05/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/934,495	MAMADA, NOBUO	
	Examiner	Art Unit	
	John L. Goff	1733	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22 and 41-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22 and 41-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/441,960.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/23/04 has been entered.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

3. Claims 22 and 41-49 are rejected under 35 U.S.C. 102(e) as being anticipated by Blackadar et al. (U.S. Patent 6,336,365).

Blackadar et al. disclose an accelerometer, i.e. an electronic circuit in which applied voltages are varied. Blackadar et al. teach a circuit board (710) comprising a front surface and a back surface and lands (704) formed on each surface at substantially plane-symmetrical positions, every two lands are connected to each other by a conductor through hole (702) (See Figure 7). Blackadar et al. teach a multilayer capacitor (708) (e.g. a transducer) comprising a body having dielectric layers (706) and internal electrode layers (P1A, P2A) and a pair of terminal electrodes (714a, 714b) formed on two sides of the body, the dielectric layers and internal electrode layers are connected to the terminal electrodes in a parallel, alternate manner

(See Figure 7 and Column 13, lines 19-22). Blackadar et al. teach mounting a first multilayer capacitor (404a) on the lands of the front surface of the circuit board and a second multilayer capacitor (404b) on the lands of the back surface of the circuit board, the first and second multilayer capacitors coupled through the conductor through hole, to form an accelerometer (Figure 6A-6C, 7, and 9 and Column 11, lines 39-45 and Column 13, lines 22-31). It is noted Blackadar et al. do not expressly disclose the first and second multilayer capacitors cancel the vibrations of each other when a voltage is applied. However, the first and second multilayer capacitors taught by Blackadar et al. are mounted on the circuit board in the same manner as that claimed by applicant and described in applicants specification such that this property is inherent in Blackadar et al.

Regarding claims 41-43, Blackadar et al. show using identical capacitors mounted on substantially symmetrical positions on the circuit board such that the length, width, height, and offset ranges required in the claims are inherent.

Regarding claim 45, Blackadar et al. show mounting identical capacitors on substantially symmetrical positions on a circuit board such that when the circuit board bends one of the capacitors is stretched and the other capacitor is compressed a corresponding amount, and thus, inherently the voltages applied during bending are the same corresponding amount, i.e. identical (Figure 9 and Column 14, lines 41-51).

Regarding claim 49, it is noted Blackadar et al. do not expressly recite the multilayer capacitors of the accelerometer as having the capability of operating at voltages having frequencies varying in the audible frequency band. However, the multilayer capacitors employed in Blackadar et al. are the same as those claimed by applicant and they are consistent

and in agreement with applicants specification (Figure 2 and Page 5, lines 22-26 and Page 6, lines 1-19) such that the multilayer capacitors taught by Blackadar et al. would inherently operate at voltages having frequencies varying in the audible frequency band.

Claim Rejections - 35 USC § 103

4. Claims 22 and 41-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blackadar et al. in view of the admitted prior art (Specification pages 1 and 2).

In the event the multilayer capacitors taught by Blackadar et al. do not inherently vibrate or operate at voltages having frequencies varying in the audible frequency band the following rejection is set forth.

Blackadar et al. is described in full detail above in paragraph 3. However, as to claims 22 and 49, Blackadar et al. do not expressly teach that the multilayer capacitors of the accelerometer vibrate and have the capability of operating at voltages having frequencies varying in the audible frequency band. However, Blackadar et al. are not limited to any particular multilayer capacitor such that it would have been obvious to one of ordinary skill in the art at the time the invention was made to use as the multilayer capacitor taught by Blackadar et al. any well known and conventional multilayer capacitor used in the electronic devices art such as that shown for example by the admitted prior art as only the expected results would be achieved.

The admitted prior art is directed to mounting a multilayer capacitor on the front surface of a circuit board. The admitted prior art teaches that the multilayer capacitor produces vibrations that cause the circuit board to resonate with the vibrations and produce audible sounds (Specification pages 1 and 2).

Response to Arguments

5. Applicant's arguments with respect to claims 22 and 41-49 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues, "1) Blackadar et al. disclose that every two plane-symmetrical supports (not shown) of a pair of opposite transducers 404a and 404b disposed on a flexible beam 302 may not be connected with each other so that the neutral axis 418 is not significantly affected and therefore does not pass through either of the transducers 404a and 404b, while the present invention employs that every two lands at plane-symmetrical positions in two capacitors are connected to each other to cancel out vibrations generated from the capacitor;"

Blackadar et al. show mounting multilayer capacitors on substantially symmetrical positions on a circuit board (See Figures 6A-6C and 9). Furthermore, Blackadar et al. show the manner in which a multilayer capacitor is connected to a circuit board (Figure 7), the multilayer capacitor being connected to a pair of lands with the pair of lands connected to another substantially plane-symmetrical pair of lands through a conductor through hole. Thus, clearly Blackadar et al. "employs that every two lands at plane-symmetrical positions in two capacitors are connected to each other".

Applicant further argues, "(2) Blackadar el al. disclose a method for detecting whether the flexible circuit board 302 is bent or not by using one or more transducers 404, 404a and 404b with a piezoceramic dielectric therein in order to detect the acceleration of an object on the flexible circuit board while, the present invention is directed to a method for mounting capacitors on the lands on a circuit board in order to cancel out vibrations generated by the capacitors;"

As noted above, Blackadar et al. do not expressly disclose the first and second multilayer capacitors cancel the vibrations of each other when a voltage is applied. However, the first and second multilayer capacitors taught by Blackadar et al. are mounted on the circuit board in the same manner as that claimed by applicant and described in applicants specification such that this property is inherent in Blackadar et al.

Applicant further argues, "(3) Blackadar et al. detect electrical signals, i.e. voltages, generated from the transducer by mechanical deformation therein. The present invention, however, applies the voltages with the audible frequency to two symmetrically-positioned capacitors, respectively, to obtain required capacitance therefrom while reducing noises therefrom;"

The claims are not commensurate in scope with this argument.

Applicant further argues, "(4) Blackadar et al. may use one or more transducer 404 (or 404a and 404b) to detect the bending of the flexible circuit board 302, while the inventive method may not be implemented by one capacitor but must mount two symmetrical capacitors and two symmetrical lands on a circuit board at substantially plane-symmetrically to cancel out vibrations generated from the capacitor, as defined in claims 22, 28, and 35."

Blackadar et al. show mounting two multilayer capacitors on substantially symmetrical lands on a circuit board (See Figures 6A-6C and 9).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **John L. Goff** whose telephone number is **(571) 272-1216**. The examiner can normally be reached on M-F (7:15 AM - 3:45 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Crispino can be reached on (571) 272-1226. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John L. Goff
May 13, 2004

JEFF H. AFTERGUT
PRIMARY EXAMINER
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